IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Minerva M. Yeung et al.

Application No.: 10/774,178

Filed: February 6, 2004

For: METHODS FOR SAVING ENERGY CONSUMPTION OF BUFFERED REAL TIME MULTIMEDIA APPLICATIONS ON SIMULTANEOUS MULTI-THREADING PROCESSORS

Examiner: Arcos, Caroline H.

Art Group: 2195

Confirmation No.: 7185

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Assistant Commissioner For Patents
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APPEAL BRIEF
IN SUPPORT OF APPELLANTS' APPEAL
TO THE BOARD OF PATENT APPEALS

Applicants (hereinafter "Appellants") hereby submit this Brief in support of an Appeal from a decision of a final Office Action mailed April 27, 2010. Appellants respectfully request consideration of the accompanying Appeal by the Board of Patent Appeals for allowance of the invention as presently recited in the claims.

TABLE OF CONTENTS

I. REAL PARTY IN INTEREST

The real party in interest of the above-referenced U.S. Patent application is Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California, 95052, to whom the application has been assigned.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellants' knowledge, there are no prior or pending appeals, interferences, or judicial proceedings related to the subject matter of this appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 7, 10-15, 19, 39, 40, 44 and 44-49 are pending in the above-referenced application.

Claims 1-4, 7, 10-15, 19, 39, 40, 44 and 44-49 were finally rejected in the final Office Action mailed April 27, 2010. These claims are the subject of this Appeal.

IV. STATUS OF AMENDMENTS

In response to the final Office Action mailed April 27, 2010, Appellants filed an After Final Response on June 28, 2010.

An Advisory Action was mailed on July 20, 2010, to which Appellants filed a Notice of Appeal and Pre-appeal Brief Request for Review.

The Panel Decision was mailed on August 10, 2010.

A Supplemental Amendment was filed concurrently but separately from this Appeal Brief under 37 C.F.R. §§ 41.47(c)(2), 41.33(b)(1)-(b)(2) and M.P.E.P. § 1206. In the Supplemental Amendment, claims 44 and 46-49 are cancelled.

A copy of all claims on appeal is attached hereto as Appendix A.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The claims are summarized as follows. In the summary below, the referenced portion of the Specification should be construed as only representative of the teachings that support the claimed feature(s). Thus, the cited portions are sufficient to support the claim, but are not necessarily the exclusive support in the Specification for such claim features.

1. A method, comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system; (paragraph [0021]; application states are discussed in paragraph [0022])

determining availability of a processor to perform simultaneous multi-threading and the buffer; (paragraph [0028])

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer; (paragraph [0049])

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; (paragraphs [0055] and [0063]) and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads. (paragraph 0032])

14. A computer readable storage medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system; (paragraph [0021]; application states are discussed in paragraph [0022])

determining availability of a processor to perform simultaneous multi-threading and the buffer; (paragraph [0028])

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer; (paragraph [0049])

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; (paragraphs [0055] and [0063]) and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads. (paragraphs [0055] and [0063])

39. A system, comprising:

a memory to store data and instructions; (paragraph [0017])

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor to include a bus unit to receive a sequence of instructions from said memory; (paragraph [0017])

an execution unit coupled to said bus unit, said execution unit to execute said sequence of instructions, said sequence of instructions to cause said execution unit to: (paragraphs [0017]-[0018])

monitor a state of a multi-threaded application running in a system buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system; (paragraph [0021]; application states are discussed in paragraph [0022])

determine availability of a processor to perform simultaneous multi-threading and the buffer; ; (paragraph [0028])

coordinate dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer; (paragraph [0049])

dynamically adjust one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; (paragraphs [0055] and [0063]) and

dynamically adjust the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads. (paragraphs [0055] and [0063])

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-4, 7, 10-15, 19 and 39-40 were rejected under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Appellants regard as the invention.

Claims 1, 11-14, 19, and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0115428 of Zaccarin et al. (hereinafter "Zaccarin"), in view of U.S. Patent Application Publication No. 2001/0056456 of Cota-Robles (hereinafter "Cota-Robles").

Claims 2-4, 15, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles, and further in view of U.S. Patent No. 6,662,203 of Kling et al., (hereinafter "Kling").

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles as applied to claim 1 above, and further in view of U.S. Patent No. 4,811,208 of Myers et al., (hereinafter "Myers").

Claim 10 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles and Myers, as applied to claim 7 above, and further in view of U.S. Patent Application Publication No. 2002/0188884 of Jain et al (hereinafter "Jain").

VII. ARGUMENT

REJECTIONS UNDER 35 U.S.C. § 112

Claims 1-4, 7, 10-15, 19, and 39-40 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the invention.

Claims 1, 14 and 39 were rejected under 35 U.S.C. § 112, second paragraph because the Examiner asserts that it is unclear what is meant by "state of multi-threaded application." Appellants contend that one possessing the ordinary level of skill in the pertinent art at the time the invention was made would interpret "state of application" to clearly describe what the application may be doing at an observed time.

The above claims were also rejected under 35 U.S.C. § 112, second paragraph because the Examiner asserts that it is unclear what is the relation between the limitations "monitoring the state of the multi-threaded application" and "[monitoring] the buffer." Appellants point out that the independent claims recite that said buffer is associated with the application. Thus, Appellants contend that because the buffer is associated with the application, the state of the buffer and the state of the application are clearly related. Therefore, the rejections of the independent claims under 35 U.S.C. § 112, second paragraph are improper for at least the reasons above.

REJECTIONS UNDER 35 U.S.C. § 103: Claims 1-2, 5-7, 9, 11-13, 15 and 17-20

Claims 1, 11-14, 19, and 39 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Application Publication No. 2003/0115428 of Zaccarin et al. (hereinafter

"Zaccarin"), in view of U.S. Patent Application Publication No. 2001/0056456 of Cota-Robles (hereinafter "Cota-Robles").

Appellants respectfully contend that these claims are not rendered obvious by the cited references for at least the following reason: the references, alone and in combination, disclose adjusting a buffer size.

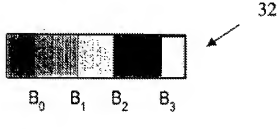
Claim 1 recites dynamically **adjusting a buffer size** based, at least in part, on an adjusted voltage or frequency applied to a processor and the coordination of the dispatch of threads. Independent claims 14 and 39 recite similar features.

The Examiner has cited paragraphs [0015], [0017] and [0019] to disclose the above features of the independent claims. Appellants point the Zaccarin clearly discloses a fixed buffer than cannot be adjusted.

Paragraph [0019] of Zaccarin discloses:

> For clarity, the variables B.sub.0, B.sub.1, B.sub.2 and B.sub.3 in both FIGS. 2 and 3 are represented as being static. **The overall buffer size of the buffer block 32 is similarly fixed**.

Variables B.sub.0-B.sub.3 represent buffer levels, as described in paragraph [0018] of the reference. Paragraph [0019] of Zaccarin disclose that in alternative embodiments, B.sub.0-B.sub.3 may change; however, it is clear from the disclosures of the reference that the buffer size of the buffer measured by said variables is always fixed. Appellants point out that FIG. 3 of Zaccarin appears as follows:



Even if it is assumed for the sake of argument that Zaccarin discloses adjusting processor operating conditions based on these variables (i.e., assuming processing operating conditions exist for buffer levels B.sub.0-B.sub.3), and that said variables (buffer levels) may be changed, Appellants contend that the size of buffer 32 is still fixed, and cannot be changed. In contrast, the independent claims as amended recite **adjusting a buffer size** based, at least in part, on an adjusted voltage or frequency applied to a processor and the coordination of the dispatch of threads. Therefore, Zaccarin cannot be cited to disclose the above feature of the independent claims.

Cota-Robles fails to cure the defects of Zaccarin as Cota-Robles contains no disclosures directed towards adjusting a buffer size based, at least in part, on an adjusted voltage or frequency applied to a processor and the coordination of the dispatch of threads. Therefore, no combination of Zaccarin and Cota-Robles discloses the above feature of the independent claims.

The Examiner has failed to establish a *prima facie* case of obviousness because no combination of the references cited by the Examiner discloses all of the elements of the independent claims. Therefore, the Examiner's rejection of the independent claims is improper for failing to include a proper rejection of the independent claims, as set forth in case law cited in section 706.02(j) of the MPEP: "[t]o support the conclusion that the claimed invention is directed to obvious subject matter . . . the references must expressly or impliedly suggest the claimed invention." *Ex parte Clapp*, 227 USPQ 972, 973 (Bd. Pat. App. & Inter. 1985).

Claims 2-4, 15, and 40 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles, and further in view of U.S. Patent No. 6,662,203 of Kling et al., (hereinafter "Kling"). The deficiencies of Zaccarin and Cota-Robles with respect to independent claims 1, 14 and 39 are discussed above. Kling fails to cure the above deficiencies

of Zaccarin and Cota-Robles, as Kling contains no disclosures directed towards the limitations of the independent claims discussed above. Therefore, no combination of Zaccarin, Cota-Robles and Kling may be cited to disclose the independent claims. Each of claims 2-4, 15 and 40 depend from one of the independent claims discussed above. Per the guidelines set forth by the Federal Circuit in *In re Fine*, 837 F.2d 1071, (Fed.Cir. 1988), claims that depend from nonobvious independent claims are likewise nonobvious over the references.

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles as applied to claim 1 above, and further in view of U.S. Patent No. 4,811,208 of Myers et al., (hereinafter "Myers"). The deficiencies of Zaccarin and Cota-Robles with respect to independent claim 1 are discussed above. Myers fails to cure the above deficiencies of Zaccarin and Cota-Robles, as Myers contains no disclosures directed towards the limitations of independent claim 1 discussed above. Therefore, no combination of Zaccarin, Cota-Robles and Myers may be cited to disclose independent claim 1. Claim 10 depends from independent claim 1. Per the guidelines set forth by the Federal Circuit as discussed above, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

Claim 10 was also rejected under 35 U.S.C. § 103(a) as being unpatentable over Zaccarin in view of Cota-Robles and Myers, as applied to claim 7 above, and further in view of U.S. Patent Application Publication No. 2002/0188884 of Jain et al (hereinafter "Jain"). The deficiencies of Zaccarin, Cota-Robles and Myers with respect to independent claim 1 are discussed above. Jain fails to cure the above deficiencies of Zaccarin, Cota-Robles and Myers, as Jain contains no disclosures directed towards the limitations of independent claim 1 discussed above. Therefore, no combination of Zaccarin, Cota-Robles, Myers and Jain may be cited to

disclose independent claim 1. Claim 10 depends from independent claim 1. Per Per the guidelines set forth by the Federal Circuit discussed above, claims that depend from nonobvious independent claims are likewise nonobvious over the references.

VIII. CONCLUSION

In conclusion, Appellants respectfully submit that all appealed claims in this application are patentable and requests that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims.

A single copy of this brief is submitted as per 37 C.F.R. §41.37(a). The fee of $540.00 to cover the filing of an Appeal Brief for one other than a small entity as specified in 37 C.F.R. §1.17(c) is submitted herewith. Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,
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Date: October 29, 2010

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IX. CLAIMS APPENDIX

1. (Previously Presented) A method, comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determining availability of a processor to perform simultaneous multi-threading and the buffer;

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

2. (Previously Presented) The method of claim 1, wherein coordinating dispatch of the threads of the multi-threaded application includes assessing execution readiness of the one or more activities of each thread.

3. (Previously Presented) The method of claim 2, wherein coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

4. (Previously Presented) The method of claim 3, wherein a first activity is delayed from being dispatched to wait for a second activity to be ready so that both the first and second activities are dispatched together, and wherein the first and second activities are from one or more applications.

5-6. (Cancelled).

7. (Previously Presented) The method of claim 1, further comprising

determining the availability of configurable hardware components including an arithmetic logic unit (ALU), and registers in the system, wherein coordinating dispatch of the threads of the multi-threaded application is further based on the availability of the configurable hardware components.

8-9. (Cancelled)

10. (Previously Presented) The method of claim 7, wherein adjusting the voltage applied to the processor includes powering on or powering off at least a portion of circuitry in the system.

11. (Previously Presented) The method of claim 1, wherein monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer.

12. (Previously Presented) The method of claim 11, wherein monitoring the buffer fullness levels includes comparing the buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

13. (Previously Presented) The method of claim 12, wherein comparing the buffer level includes determining buffer overflow and buffer underflow conditions based, at least in part, on the high level mark and the low level mark.

14. (Previously Presented) A computer readable storage medium containing executable instructions which, when executed in a processing system, causes the processing system to perform a method comprising:

monitoring a state of a multi-threaded application running in a system and a buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determining availability of a processor to perform simultaneous multi-threading and the buffer;

coordinating dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer;

dynamically adjusting one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; and

dynamically adjusting the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

15. (Previously Presented) The computer readable storage medium of claim 14, wherein coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

16-18. (Cancelled)

19. (Previously Presented) The computer readable storage medium of claim 14,

wherein monitoring the buffer associated with the multi-threaded application includes monitoring buffer fullness levels of the buffer, and wherein monitoring the buffer fullness levels includes comparing the buffer level with predetermined buffer fullness levels, wherein the predetermined buffer fullness levels include a high level mark and a low level mark.

20-38. (Cancelled)

39. (Previously Presented) A system, comprising:

a memory to store data and instructions;

a processor coupled to said memory on a bus, said processor operable to perform instructions, said processor to include a bus unit to receive a sequence of instructions from said memory;

an execution unit coupled to said bus unit, said execution unit to execute said sequence of

instructions, said sequence of instructions to cause said execution unit to:

monitor a state of a multi-threaded application running in a system buffer associated with the multi-threaded application, wherein each thread includes one or more activities to be executed by the system;

determine availability of a processor to perform simultaneous multi-threading and the buffer;

coordinate dispatch of threads of the multi-threaded application to increase execution overlap of activities executing in the system based, at least in part, on the availability of the buffer;

dynamically adjust one or more of the frequency or the voltage applied to the processor based, at least in part, on the availability of the buffer and the coordination of the dispatch of the threads; and

dynamically adjust the buffer size based, at least in part, on the adjusted voltage or frequency applied to the processor and the coordination of the dispatch of the threads.

40. (Previously Presented) The system of claim 39, wherein said coordinating dispatch of the threads of the multi-threaded application includes delaying a ready-to-be-dispatched activity from being dispatched.

41-43. (Cancelled)

44. (Previously Presented) A system, comprising:

a multi-threading processor; and

a resource manager coupled to the multi-threading processor, the resource manager is to monitor states of a multi-threaded application running in the system, the states of the application including buffer fullness levels of one or more buffers used by the application, the resource manager is to further monitor states of the threads of the application in the system for execution readiness, wherein the resource manager is to

increase or decrease resources available in the system depending on the state of the application and/or the states of the threads in the system, and.

change the execution readiness of a thread from a ready state to a queued state to increase subsequent thread execution overlap with execution of another thread based, at least in part, on the buffer fullness levels.

45. (Cancelled).

46. (Previously Presented) The system of claim 45, wherein the resource manager is to further change the execution readiness of a thread from a ready state to a queued state to increase subsequent system idle time when there is no thread execution.

47. (Original) The system of claim 46, wherein the resource manager is to increase or decrease the resources available in the system to avoid buffer underflow or overflow conditions to occur to the one or more buffers.

48. (Previously Presented) An apparatus, comprising:

a processor capable of simultaneous multi-threading , the processor having logic to monitor states of a multi-threaded application running in a system, the states of the application including buffer fullness levels of one or more buffers used by the application;

logic to monitor states of the threads of the application in the system for execution readiness;

logic to adjust resources available in the system depending on the state of the application and/or the states of the threads in the system and to adjust the available resources in the system includes logic to determine if the buffer fullness levels of one or more buffers are in a critical stage; and

a memory to store the logic.

49. (Original) The apparatus of claim 48, further comprising:

logic to change the execution readiness of a thread from a ready state to a queued state when it is determined that there is no other thread running or ready to be dispatched.

50. (Cancelled).

X. EVIDENCE APPENDIX

None.

XI. RELATED PROCEEDINGS APPENDIX

None.